PGA2310 Stereo Audio Volume Control

1 Features

- Digitally-Controlled Analog Volume Control:
  - Two Independent Audio Channels
  - Serial Control Interface
  - Zero Crossing Detection
  - Mute Function
- Wide Gain and Attenuation Range: 31.5 dB to −95.5 dB With 0.5-dB Steps
- Low Noise and Distortion:
  - 120-dB Dynamic Range
  - 0.0004% THD+N at 1 kHz
- Low Interchannel Crosstalk: −126 dBFS
- Noise-Free Level Transitions
- Power Supplies: 15-V Analog, 5-V Digital
- Available in DIP−16 and SOL−16 Packages
- Pin and Software Compatible With the PGA2311 and Cirrus Logic CS3310™

2 Applications

- Audio Amplifiers
- Mixing Consoles
- Multi-Track Recorders
- Broadcast Studio Equipment
- Musical Instruments
- Effects Processors
- A/V Receivers
- Car Audio Systems

3 Description

The PGA2310 is a high-performance, stereo audio volume control designed for professional and high-end consumer audio systems. The ability to operate from ±15-V analog power supplies enables the PGA2310 to process input signals with large voltage swings, thereby preserving the dynamic range available in the overall signal path. Using high performance operational amplifier stages internal to the PGA2310 yields low noise and distortion, while providing the capability to drive 600-Ω loads directly without buffering. The three-wire serial control interface allows for connection to a wide variety of host controllers, in addition to support for daisy-chaining multiple PGA2310 devices.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PGA2310	SOIC (16)	7.50 mm × 10.30 mm
	PDIP (16)	6.35 mm × 19.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Stereo Audio Volume Control

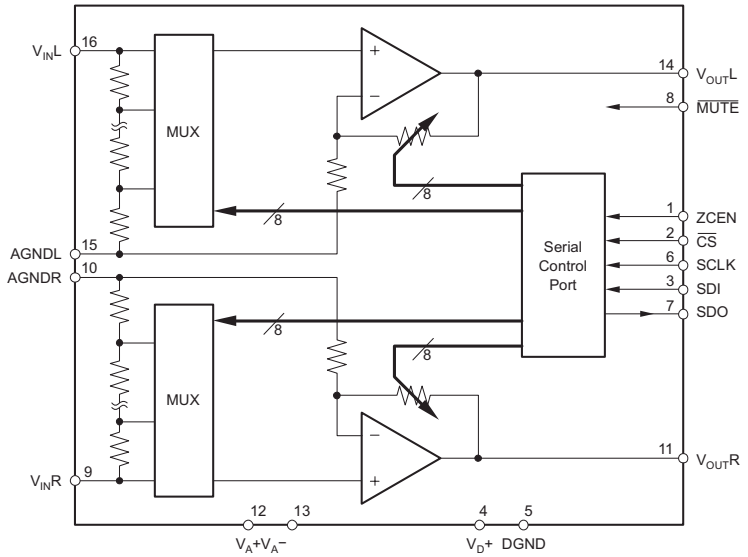


Table of Contents

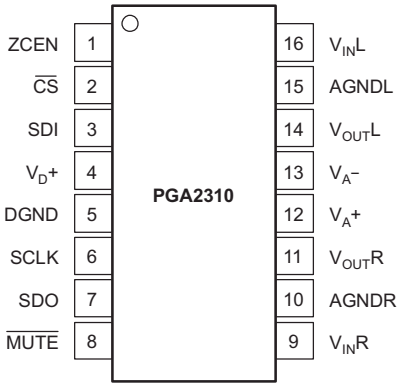
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2004) to Revision C	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

5 Pin Configuration and Functions

D and P Pakcages
16 Pins SOIC and PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	ZCEN	I	Zero Crossing Enable Input (Active High)
2	$\overline{CS}$	I	Chip Select Input (Active Low)
3	SDI	I	Serial Data Input
4	V_D+	I	Digital Power Supply, 5 V
5	DGND	—	Digital Ground
6	SCLK	I	Serial Clock Input
7	SDO	O	Serial Data Output
8	$\overline{MUTE}$	I	Mute Control Input (Active Low)
9	V_{IN}R	I	Analog Input, Right Channel
10	AGNDR	—	Analog Ground, Right Channel
11	V_{OUT}R	O	Analog Output, Right Channel
12	V_A+	I	Analog Power Supply, 15 V
13	V_A–	I	Analog Power Supply, –15 V
14	V_{OUT}L	O	Analog Output, Left Channel
15	AGNDL	—	Analog Ground, Left Channel
16	V_{IN}L	I	Analog Input, Left Channel

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply Voltage	V_A+		16	V
	V_A–		–16	
	V_D+		6.5	
Analog input voltage		0	V_A+,V_A–	V
Digital input voltage		–0.3	V_D+	V
Operating temperature		–55	125	°C
Junction temperature			150	°C
Lead temperature (soldering, 10 s)			300	°C
Package temperature (IR, reflow, 10 s)			235	°C
T_{stg} Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_A+	Positive analog power supply	4.5	15	15.5	V
V_A–	Negative analog power supply	–4.5	–15	–15.5	V
V_D+	Digital power supply	4.5	5	5.5	V
	Operating temperature	–55	25	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		PGA2310		UNIT
		D (SOIC)	P (PDIP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83	39.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44	26.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.5	20.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.5	10.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.2	19.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_A = 25°C, V_A+ = 15 V, V_A− = −15 V, V_D+ = 5 V, R_L = 100 kΩ, C_L = 20 pF, BW measure = 10 Hz to 20 kHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
Step Size				0.5		dB
Gain Error		Gain Setting = 31.5 dB		±0.05		dB
Gain Matching				±0.05		dB
Input Resistance				10		kΩ
Input Capacitance				7		pF
AC CHARACTERISTICS						
THD+N		V_{IN} = 10 V_{PP}, f = 1 kHz		0.0004%	0.001%	
Dynamic Range		V_{IN} = AGND, Gain = 0 dB	116	120		dB
Voltage Range, Input and Output			(VA−) + 1.5		(VA−) − 1.5	V
Output Noise		V_{IN} = AGND, Gain = 0 dB		9.5	13.5	μV_{RMS}
Interchannel Crosstalk		f = 1 kHz		–126		dBFS
OUTPUT BUFFER						
Offset Voltage		V_{IN} = AGND, Gain = 0 dB		0.5	3	mV
Load Capacitance Stability				1000		pF
Short-Circuit Current				35		mA
Unity-Gain Bandwidth, Small Signal				1.5		MHz
DIGITAL CHARACTERISTICS						
High-Level Input Voltage, V_{IH}			2		V_D+	V
Low-Level Input Voltage, V_{IL}			–0.3		0.8	V
High-Level Output Voltage, V_{OH}		I_O = 200 µA	(V_D+) − 1			V
Low-Level Output Voltage, V_{OL}		I_O = –3.2 mA			0.4	V
Input Leakage Current				1	10	µA
SWITCHING CHARACTERISTICS						
t_{SCLK}	Serial Clock (SCLK) Frequency		0		6.25	MHz
t_{PL}	Serial Clock (SCLK) Pulse Width Low		80			ns
t_{PH}	Serial Clock (SCLK) Pulse Width High		80			ns
t_{MI}	$\overline{MUTE}$ Pulse Width Low		2			ms
INPUT TIMING						
t_{SDS}	SDI Setup Time		20			ns
t_{SDH}	SDI Hold Time		20			ns
t_{CSCR}	$\overline{CS}$ Falling to SCLK Rising		90			ns
t_{CFCS}	SCLK Falling to $\overline{CS}$ Rising		35			ns
OUTPUT TIMING						
t_{CSO}	$\overline{CS}$ Low to SDO Active				35	ns
t_{CFDO}	SCLK Falling to SDO Data Valid				60	ns
t_{CSZ}	$\overline{CS}$ High to SDO High Impedance				100	ns
POWER SUPPLY						
Operating Voltage	V_A+		4.5	15	15.5	V
	V_A–		–4.5	–15	–15.5	
	V_D+		4.5	5	5.5	
Quiescent Current	I_A+	V_A+ = 15 V		7.5	10	mA
	I_A–	V_A– = –15 V		7.7	10	
	I_D+	V_D+ = 5 V		0.8	1.5	

Electrical Characteristics (continued)

At T_A = 25°C, V_A+ = 15 V, V_A− = −15 V, V_D+ = 5 V, R_L = 100 kΩ, C_L = 20 pF, BW measure = 10 Hz to 20 kHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE RANGE					
Specified Range		–40		85	°C
Operating Range		–55		125	°C

6.6 Typical Characteristics

At T_A = 25°C, V_A+ = 15 V, V_A− = −15 V, V_D+ = 5 V, R_L = 100 kΩ, C_L = 20 pF, BW measure = 10 Hz to 20 kHz, unless otherwise noted.

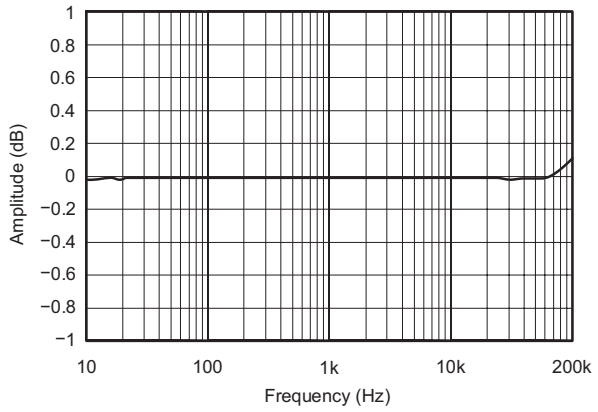


Figure 1. Frequency Response

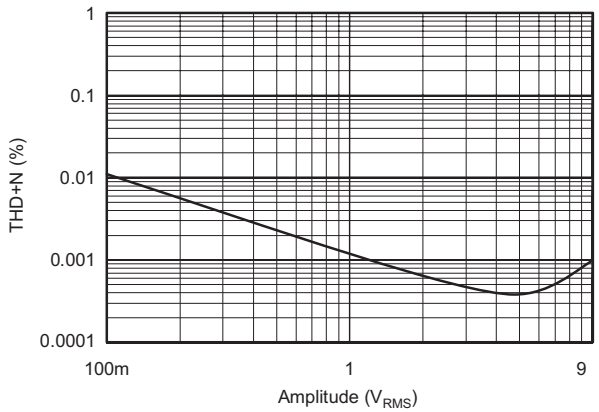


Figure 2. THD+N vs Amplitude

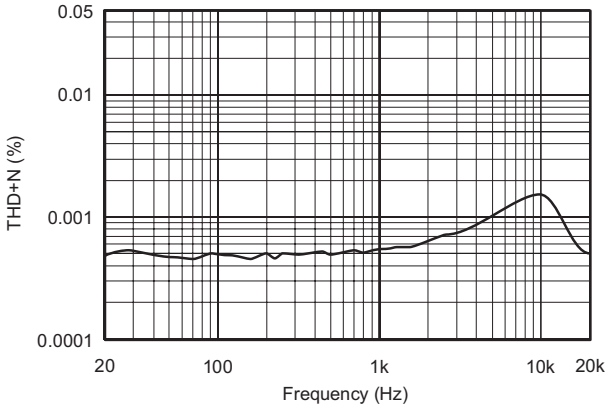


Figure 3. THD+N vs Frequency (V_{IN} = 3 V_{RMS}, Load = 100 kΩ)

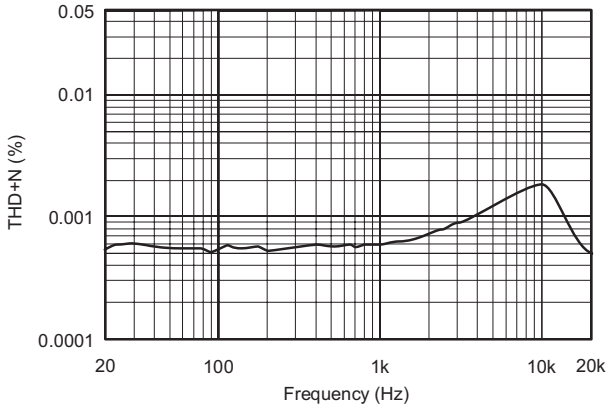


Figure 4. THD+N vs Frequency (V_{IN} = 3 V_{RMS}, Load = 600 kΩ)

Typical Characteristics (continued)

At T_A = 25°C, V_A+ = 15 V, V_A− = −15 V, V_D+ = 5 V, R_L = 100 kΩ, C_L = 20 pF, BW measure = 10 Hz to 20 kHz, unless otherwise noted.

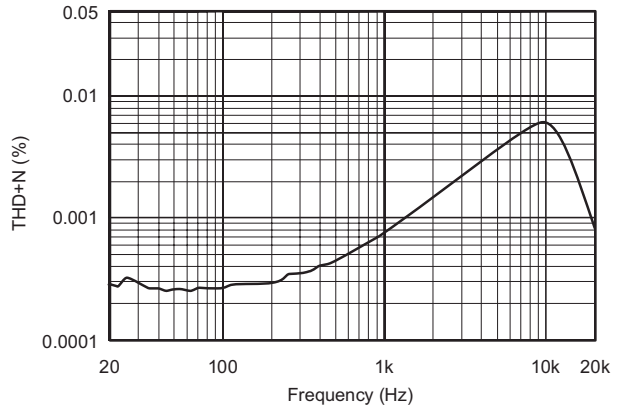


Figure 5. THD+N vs Frequency (V_{IN} = 8.5 V_{RMS}, Load = 100 kΩ)

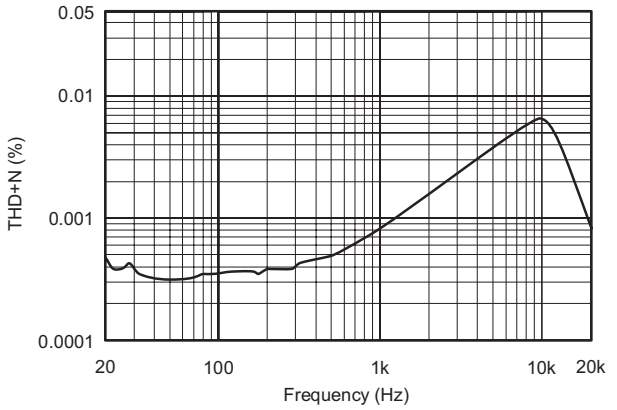


Figure 6. THD+N vs Frequency (V_{IN} = 8.5 V_{RMS}, Load = 600 kΩ)

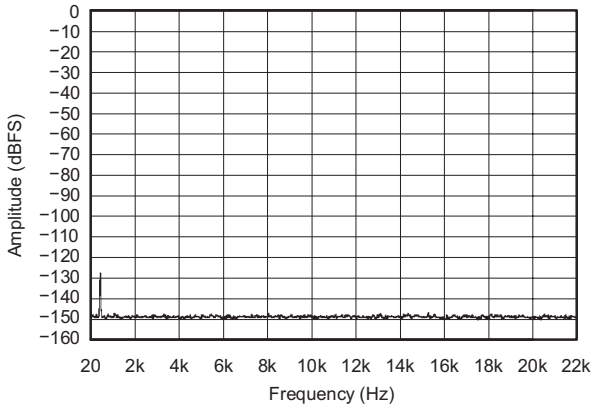


Figure 7. Amplitude vs Frequency (Crosstalk With f_{IN} = 1 kHz)

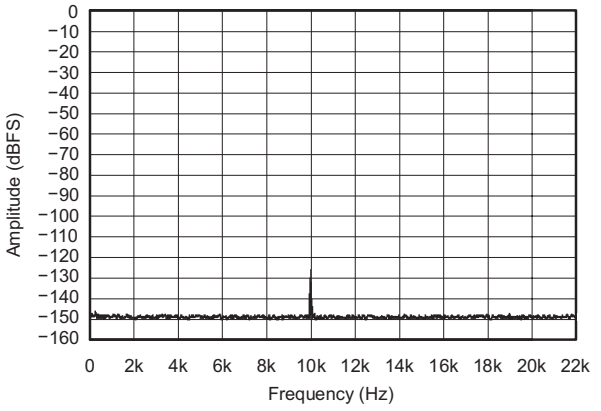


Figure 8. Amplitude vs Frequency (Crosstalk with f_{IN} = 10 kHz)

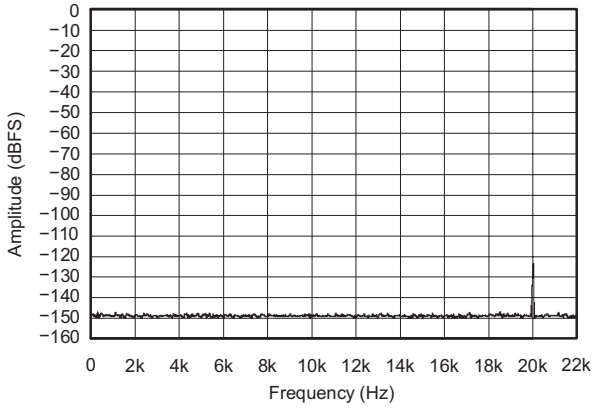


Figure 9. Amplitude vs Frequency (Crosstalk With f_{IN} = 20 kHz)

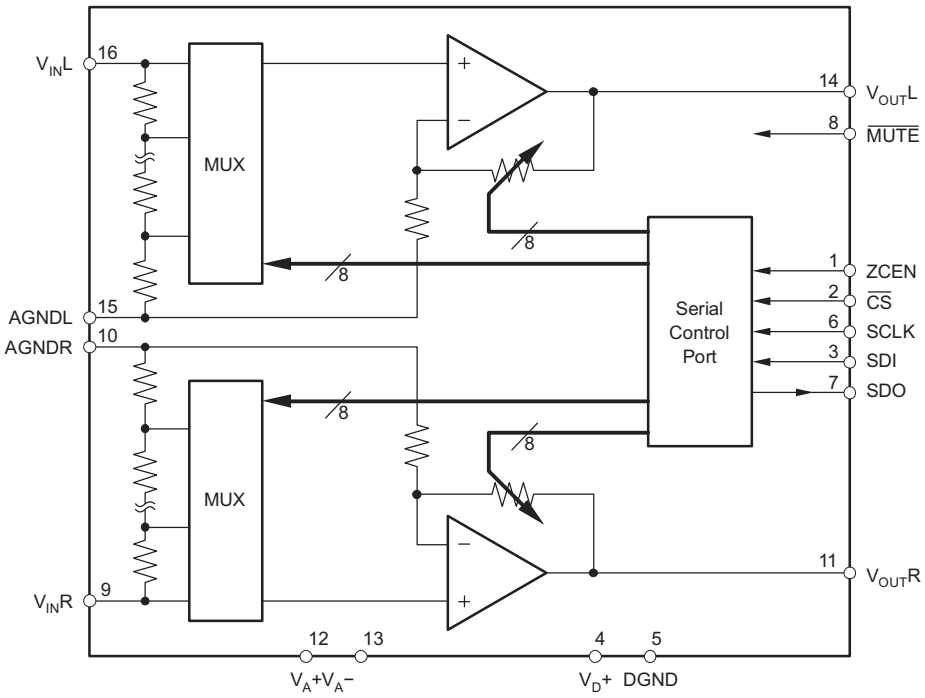
7 Detailed Description

7.1 Overview

The PGA2310 is a stereo audio volume control that can be used in a wide array of professional and consumer audio equipment. The PGA2310 is fabricated in a mixed-signal BiCMOS process for superior analog characteristics.

The heart of the PGA2310 is a resistor network, an analog switch array, and a high-performance bipolar op amp stage. The switches select taps in the resistor network that determine the gain of the amplifier stage. Switch selections are programmed using a serial control port. The serial port allows connection to a wide variety of host controllers.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Inputs and Outputs

The PGA2310 includes two independent channels, referred to as the left and right channels. Each channel has a corresponding input and output pin. The input and output pins are unbalanced, or referenced to analog ground (either AGNDR or AGNDL). The inputs are $V_{IN}R$ (pin 9) and $V_{IN}L$ (pin 16), while the outputs are $V_{OUT}R$ (pin 11) and $V_{OUT}L$ (pin 14).

The input and output pins may swing within 1.5 V of the analog power supplies, V_A+ (pin 12) and V_A- (pin 13). Given V_A+ = 15 V and V_A- = −15 V, the maximum input or output voltage range is 27 V_{PP}.

Drive the PGA2310 with a low source impedance. If a source impedance of greater than 600 Ω is used, the distortion performance of the PGA2310 begins to degrade.

7.3.2 Serial Control Port

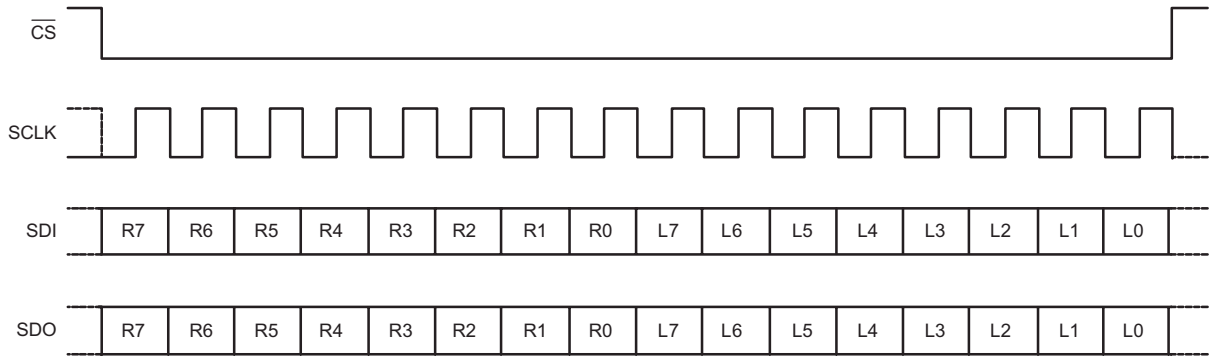
The serial control port is used to program the gain settings for the PGA2310. The serial control port includes three input pins and one output pin. The inputs include $\overline{CS}$ (pin 2), SDI (pin 3), and SCLK (pin 6). The sole output pin is SDO (pin 7).

Feature Description (continued)

The $\overline{CS}$ pin functions as the chip select input. Data may be written to the PGA2310 only when $\overline{CS}$ is low. SDI is the serial data input pin. Control data is provided as a 16-bit word at the SDI pin, 8 bits each for the left and right channel gain settings. Data is formatted as MSB first, in straight binary code. SCLK is the serial clock input. Data is clocked into SDI on the rising edge of SCLK.

SDO is the serial data output pin, and used when daisy-chaining multiple PGA2310 devices. Daisy-chain operation is described in *Daisy-Chaining Multiple PGA2310 Devices*. SDO is a tristate output, and assumes a high impedance state when $\overline{CS}$ is high.

The protocol for the serial control port is shown in Figure 10. Figure 11 shows detailed timing specifications of the serial control port.



Gain Byte Format is MSB First, Straight Binary
R0 is the Least Significant Bit of the Right Channel Gain Byte
R7 is the Most Significant Bit of the Right Channel Gain Byte
L0 is the Least Significant Bit of the Left Channel Gain Byte
L7 is the Most Significant Bit of the Left Channel Gain Byte
SDI is latched on the rising edge of SCLK.
SDO transitions on the falling edge of SCLK.

Figure 10. Serial Interface Protocol

Feature Description (continued)

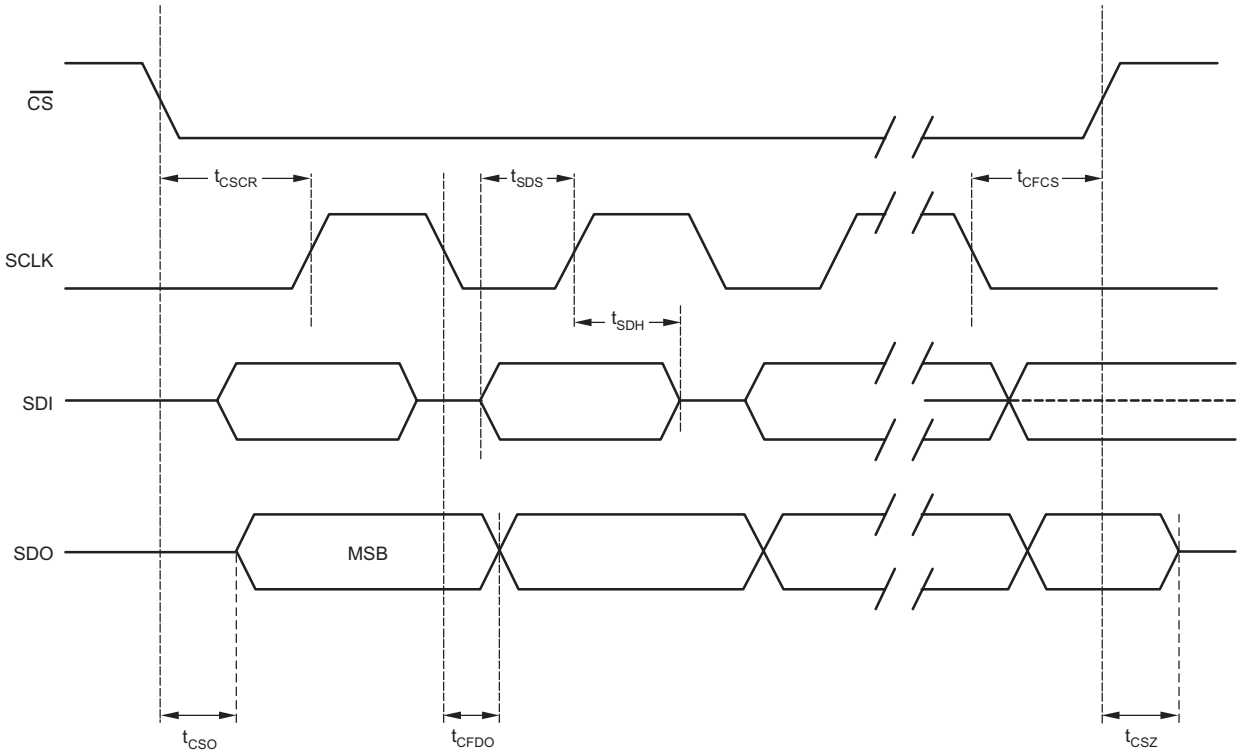


Figure 11. Serial Interface Timing Requirements

7.3.3 Gain Settings

The gain for each channel is set by its corresponding 8-bit code, either R[7:0] or L[7:0] (see Figure 10). The gain code data is straight binary format. If N equals the decimal equivalent of R[7:0] or L[7:0], then the following relationships exist for the gain settings:

- **For N = 0**: Mute Condition. The input multiplexer is connected to analog ground (AGNDR or AGNDL).
- **For N = 1 to 255**: Gain (dB) = 31.5 − [0.5 • (255 − N)]

This results in a gain range of 31.5 dB (with N = 255) to −95.5 dB (with N = 1).

Changes in gain setting may be made with or without zero crossing detection. The operation of the zero crossing detector and time-out circuitry is discussed in *Zero Crossing Detection*.

7.3.4 Daisy-Chaining Multiple PGA2310 Devices

To reduce the number of control signals required to support multiple PGA2310 devices on a printed-circuit-board, the serial control port supports daisy-chaining of multiple PGA2310 devices. Figure 12 shows the connection requirements for daisy-chain operation. This arrangement allows a three-wire serial interface to control many PGA2310 devices.

Feature Description (continued)

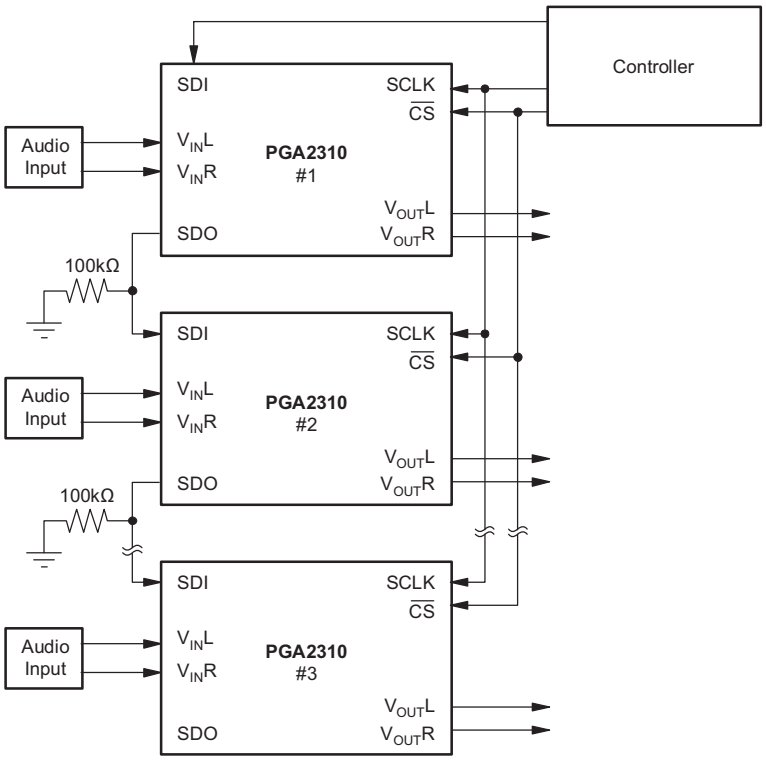


Figure 12. Daisy-Chaining Multiple PGA2310 Devices

As shown in Figure 12, the SDO pin from device 1 is connected to the SDI input of device 2, and is repeated for additional devices. This in turn forms a large shift register, in which gain data may be written for all PGA2310s connected to the serial bus. The length of the shift register is 16 × N bits, where N is equal to the number of PGA2310 devices included in the chain. The $\overline{CS}$ input must remain low for 16 × N SCLK periods, where N is the number of devices connected in the chain, to allow enough SCLK cycles to load all devices.

7.3.5 Zero Crossing Detection

The PGA2310 includes a zero crossing detection function that can provide for noise-free level transitions. The concept is to change gain settings on a zero crossing of the input signal, thus minimizing audible glitches. This function is enabled or disabled using the ZCEN input (pin 1). When ZCEN is low, zero crossing detection is disabled. When ZCEN is high, zero crossing detection is enabled.

The zero crossing detection takes effect with a change in gain setting for a corresponding channel. The new gain setting is not latched until either two zero crossings are detected, or a time-out period of 16 ms has elapsed without detecting two zero crossings. In the case of a time-out, the new gain setting takes effect with no attempt to minimize audible artifacts.

7.3.6 Mute Function

The PGA2310 includes a mute function. This function may be activated by either the $\overline{MUTE}$ input (pin 8), or by setting the gain byte value for one or both channels to 00_{HEX}. The $\overline{MUTE}$ pin may be used to mute both channels, while the gain setting may be used to selectively mute the left and right channels. Muting is accomplished by switching the input multiplexer to analog ground (AGNDR or AGNDL) with zero crossing enabled.

The $\overline{MUTE}$ pin is active low. When $\overline{MUTE}$ is low, each channel is muted following the next zero crossing event or time-out that occurs on that channel. If $\overline{MUTE}$ becomes active while $\overline{CS}$ is also active, the mute takes effect once the $\overline{CS}$ pin goes high. When the $\overline{MUTE}$ pin is high, the PGA2310 operates normally, with the mute function disabled.

7.4 Device Functional Modes

7.4.1 Power-Up State

On power up, all internal flip-flops are reset. The gain byte value for both the left and right channels are set to 00_{HEX}, or mute condition. The gain remains at this setting until the host controller programs new settings for each channel using the serial control port.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The PGA2310 is commonly used as a digitally controlled analog volume control. Analog volume is controlled through a serial interface in 0.5-dB steps, ranging from a gain of 31.5 dB down to an attenuation of −95.5 dB.

8.2 Typical Application

Figure 13 depicts the recommended connections for the PGA2310.

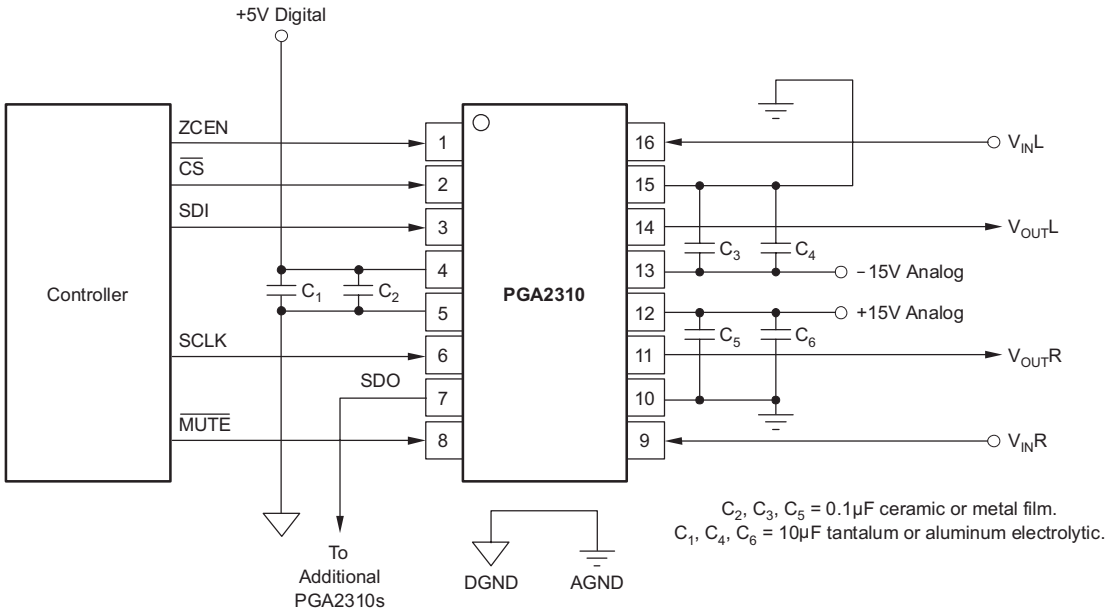


Figure 13. Recommended Connection Diagram

8.2.1 Design Requirements

- Wide dynamic range: 35.5 dB to –95.5 dB
- Operate from 5-V digital supply and ±15-V analog supplies
- Digitally controlled analog volume

8.2.2 Detailed Design Procedure

The PGA2310 is a complete digitally controlled analog stereo volume controller system on a chip requiring only a controller to select the gain or attenuation through a serial interface. Figure 13 illustrates the basic connections to the PGA2310. Power-supply bypass capacitors should be placed as close to the PGA2310 package as physically possible.

Typical Application (continued)

8.2.3 Application Curve

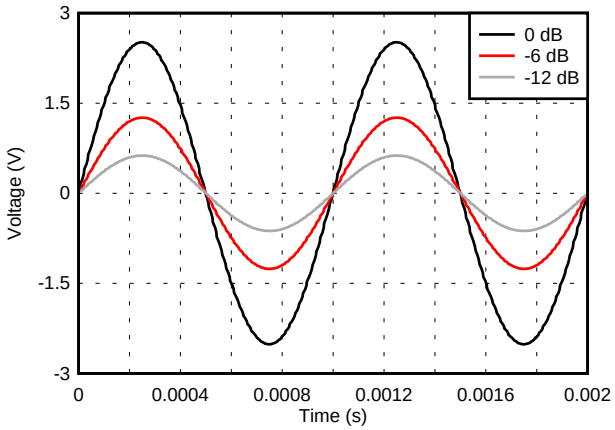


Figure 14. PGA2310 Operating at 0 dB, –6 dB and –12 dB

9 Power Supply Recommendations

The PGA2310 is specified for operation with its analog power supplies ranging from ±4.5 V to ±15.5 V and its digital power supply ranging from 4.5 V to 5.5 V.

10 Layout

10.1 Layout Guidelines

TI recommends that the ground planes for the digital and analog sections of the printed-circuit-board (PCB) be separate from one another. The planes should be connected at a single point. Figure 15 shows the recommended PCB floor plan for the PGA2310.

The PGA2310 is mounted so that it straddles the split between the digital and analog ground planes. Pins 1 through 8 are oriented to the digital side of the board, while pins 9 through 16 are on the analog side of the board.

10.2 Layout Example

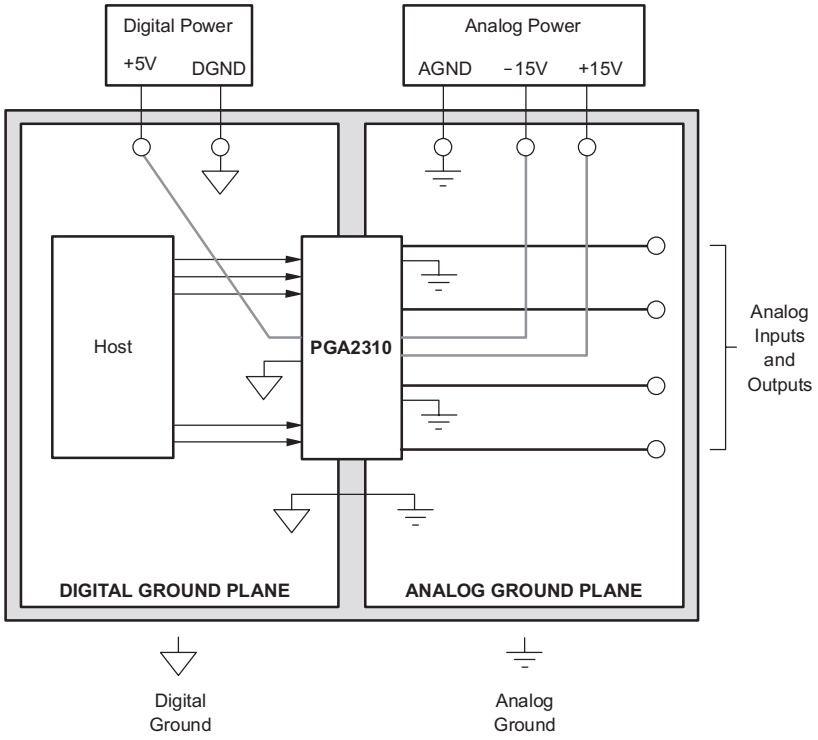


Figure 15. Typical PCB Layout Floor Plan

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For immediate development support with the PGA2310, visit Audio Amplifiers Section of the TI E2E Support Community. Here you may view previously answered questions or submit a new question to the team of application experts.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Circuit Board Layout Techniques*, SLOA089
- *Shelf-Life Evaluation of Lead-Free Component Finishes*, SZZA046
- *PGA2310-EVM: Evaluation Module User's Manual*, SBOU012

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
CS3310 is a trademark of Cirrus Logic, Inc..
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA2310PA	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	PGA2310PA	Samples
PGA2310UA	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PGA2310UA	Samples
PGA2310UA/1K	ACTIVE	SOIC	DW	16	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PGA2310UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

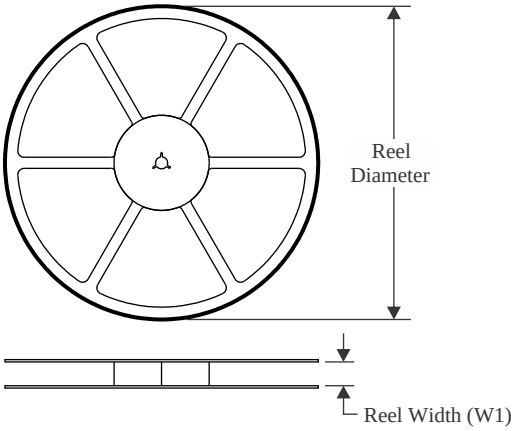
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

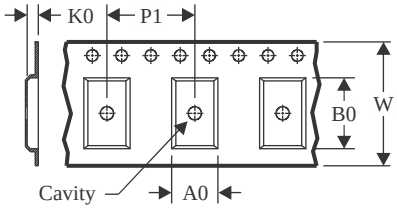
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

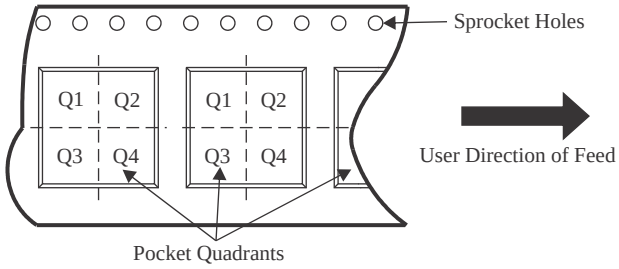


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

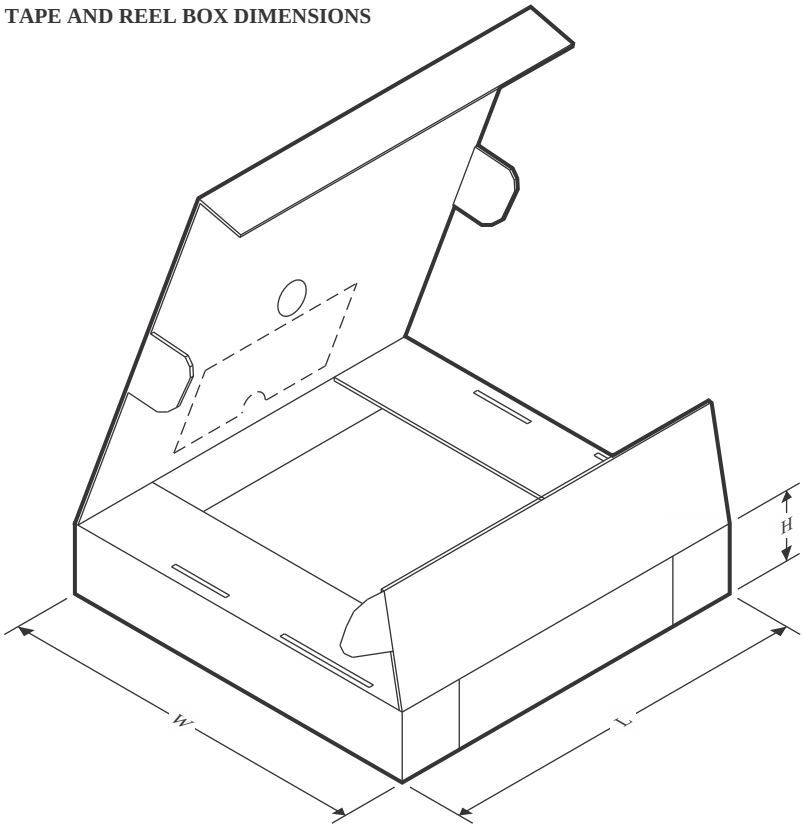
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA2310UA/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

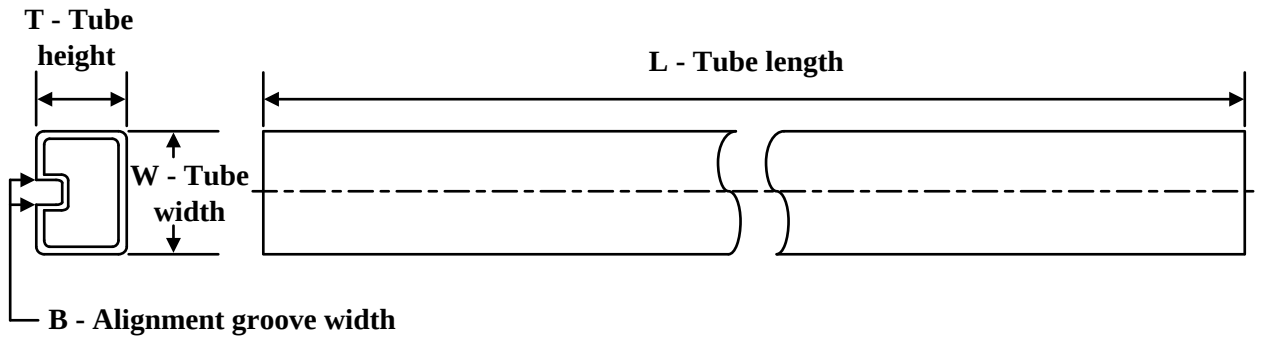
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA2310UA/1K	SOIC	DW	16	1000	356.0	356.0	35.0

TUBE



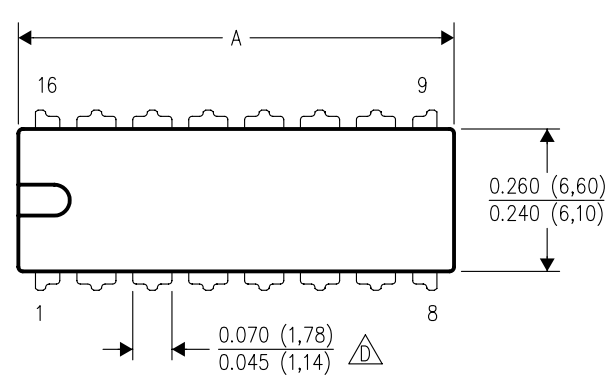
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PGA2310PA	N	PDIP	16	25	506	13.97	11230	4.32
PGA2310UA	DW	SOIC	16	40	507	12.83	5080	6.6

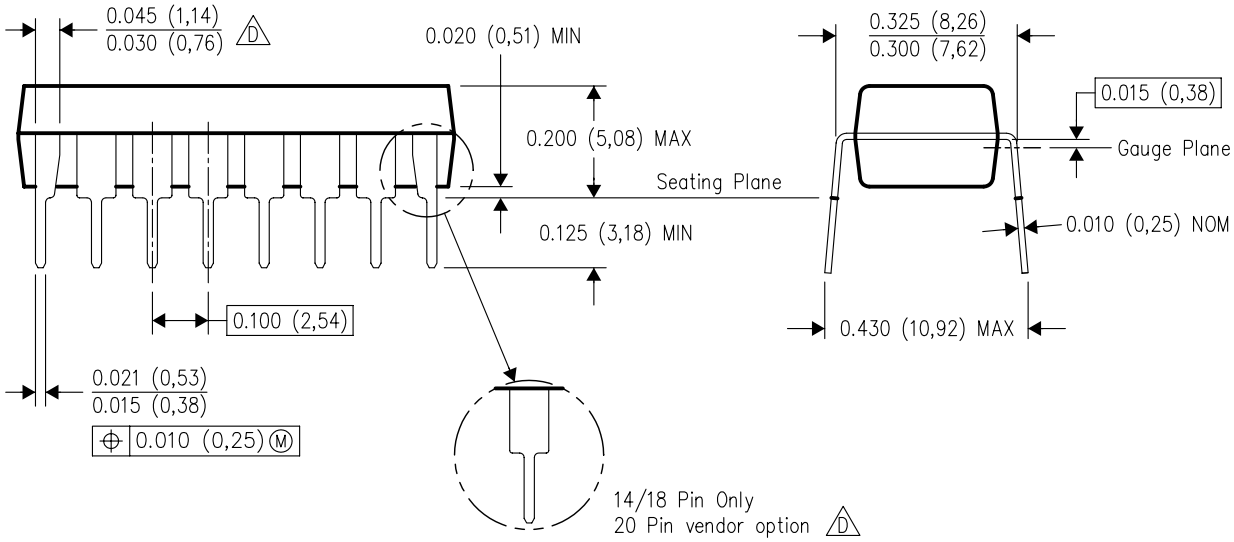
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

GENERIC PACKAGE VIEW

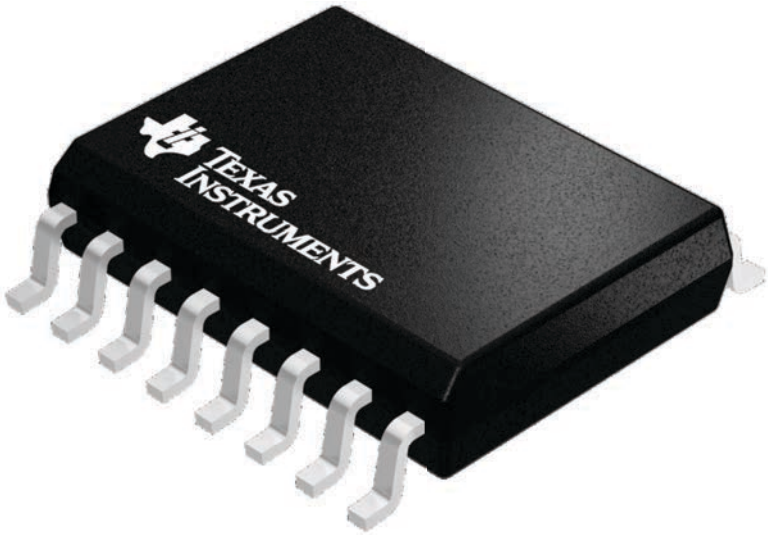
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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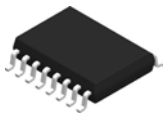
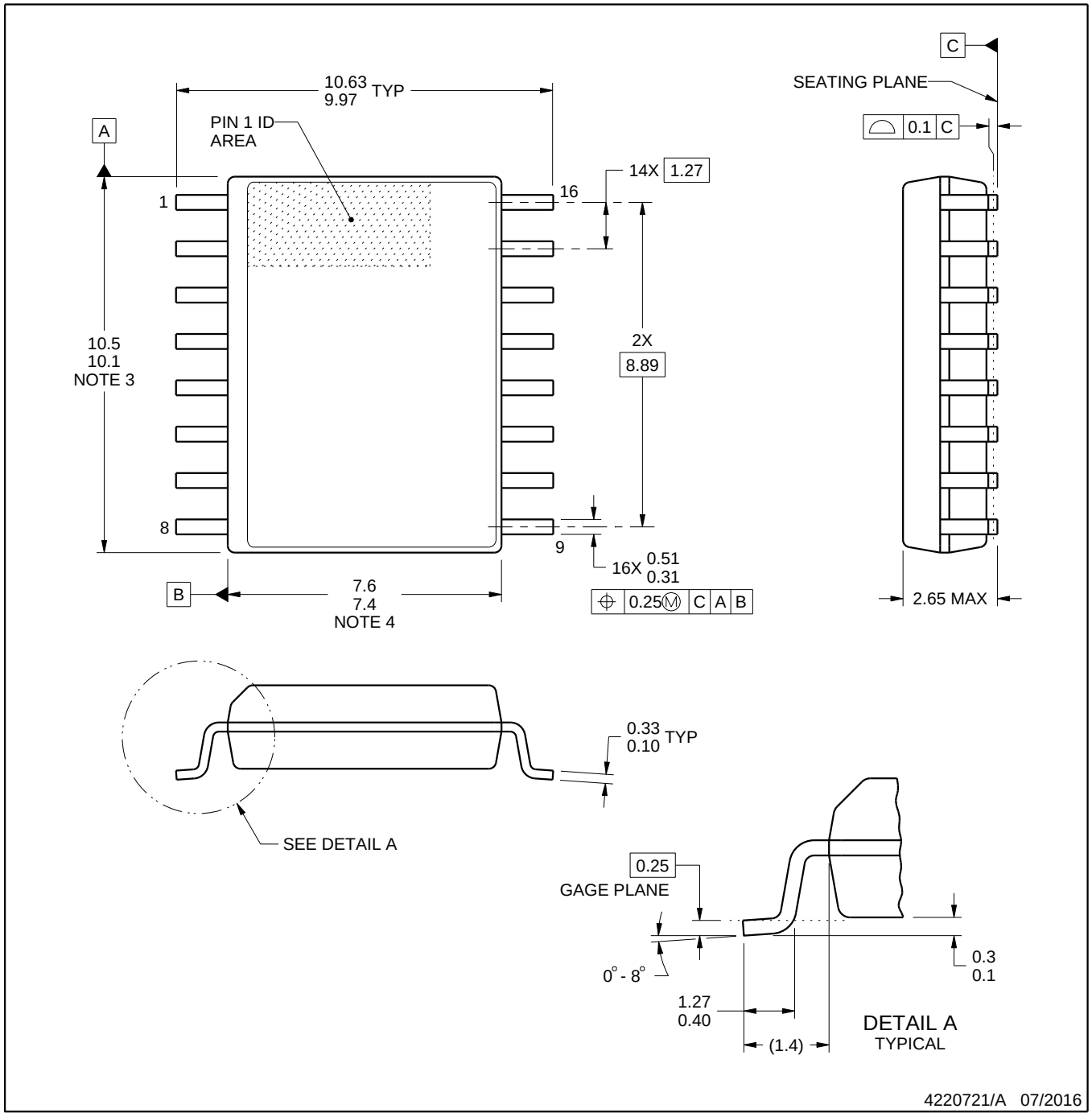


PACKAGE OUTLINE

DW0016A

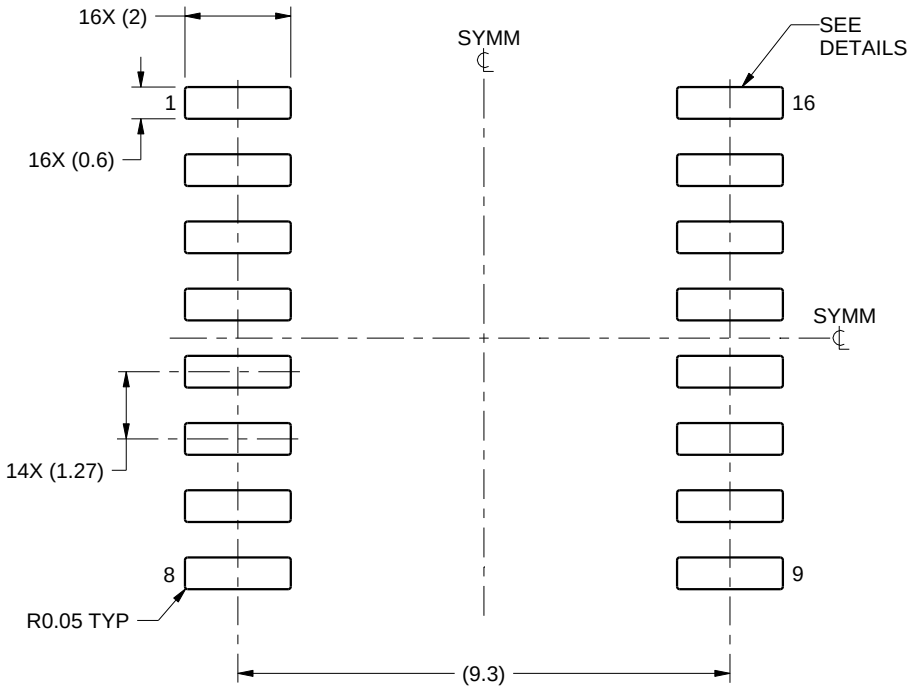
SOIC - 2.65 mm max height

SOIC

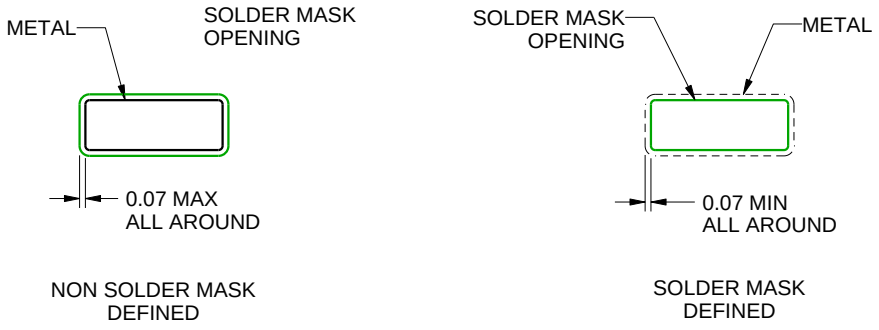


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

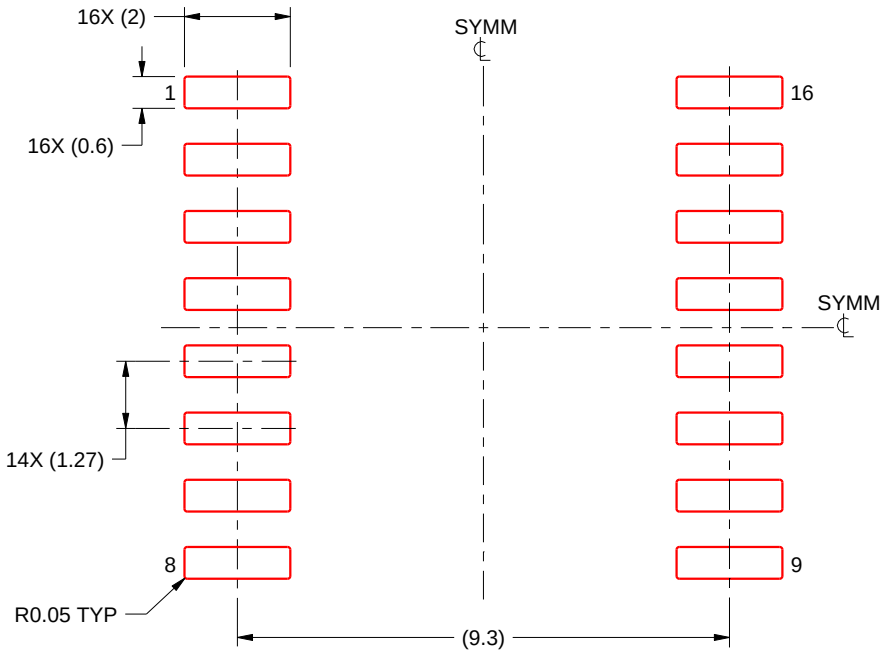


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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